Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.022”**

**.022”**

**FIELD RELIEF ELECTRODE**

**E**

**E**

**E**

**E**

**B**

**.0031”**

**.0025”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .0025” B = .0031”**

**Backside Potential: COLLECTOR**

**Mask Ref: P14**

**APPROVED BY: DK DIE SIZE .022” X .022” DATE: 9/27/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .006” P/N: 2N2946A**

**DG 10.1.2**

#### Rev B, 7/1